Form 1449 (Modified)	Atty Docket No:	U.S.
	SUNMP348	10/735,104
Information Disclosure	Applicant:	
Statement By Applicant	Xiujun Guan	
	Filing Date:	Group:
(Use Several Sheets if Necessary)	December 12, 2003	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
	A					
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					

Foreign Patent Documents

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	L							
	M							
	N							
	O							
	P							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
SKJ	Q	Hsiang-Hui Chang, Jyh-Woei Lin, Ching-Yuan Yang, Shen-Iuan Liu, "A Wide Range Delay-Locked Loop With a Fixed Latency of One Clock Cycle," IEEE Journal of Solid-State Circuits, Vol. 37, No. 8, August 2002, pp. 1021-1027
SKJ	R	Chulwoo Kim, In-Chul Hwang, Sung-Mo (Steve) Kang, "A Low-Power Small-Area ±7.28-ps-Jitter 1-GHz DLL-Based Clock Generator," IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1414-1420
	S	

Examiner	Date Considered
Suresh K Suryawanshi	4/26/06

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.